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SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
08/602,503	02/20/96	BALL M	2718US

D1M1/0115

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EXAMINER	
KIRKPATRICK,S	
ART UNIT	PAPER NUMBER
1107	

DATE MAILED: 01/15/97

Please find below a communication from the EXAMINER in charge of this application.

Commissioner of Patents

Office Action Summary	Application No. 08/602,503	Applicant(s) Ball
	Examiner Scott Kirkpatrick	Group Art Unit 1107

☐ Responsive to communication(s) filed on _____ .

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-34* is/are pending in the application.

Of the above, claim(s) *1-18* is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *19-34* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____ .

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *4*

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

This office action has been created under the Patent and Trademark Office Semiconductor Technology Quality Assurance Pilot Program. It incorporates the examination quality standards set as a result of customer focus sessions with the semiconductor industry. The listing of the field of search to follow is one of these standards.

Field of Search	Date
U.S. Class and subclass: 437/208, 209, 915	1/5/97
Other Documentation:	
Electronic data base(s):	

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-18, drawn to a device, classified in class 257, subclass 777.

   II. Claims 19-34, drawn to a method, classified in class 437, subclass 208.

2. The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the product may be made by a materially different process such as one where the stack chip is grown on the base chip rather than being attached.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with Joseph Walkowski on 1/3/97 a provisional election was made without traverse to prosecute the invention of group II, claims 19-34. Affirmation of this election must be made by applicant in responding to this Office action. Claims 1-18 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 19 and 20 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Kuroda.

7. Claims 19 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Kuranaga.

Kuranaga teaches back to back semiconductor dies mounted on another chip, which can be considered another substrate attaching the stacked chip by wire bonding, and a third chip mounted on the stack chip.

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 21-29, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Kuranaga and Kuroda as applied to claim 19 and 20 and further in view of Fogal et al.

Kuroda fails to teach subsequent chips mounted on the first stacked chip.

Kuranaga teaches a subsequent chip mounted on the first stacked chip, but fails to teach the chip connected to the substrate, rather, flip chip connected to the chip immediately below. Kuranaga and Kuroda also fail to teach discrete components added.

Fogal teaches attaching discrete components to chips, substrates, stacking multiple chips, and attaching multiple chips and discrete components to both other chips and the substrate by wire bonding. Fogal fails to teach a chip mounted face down to the substrate with a chip mount face up to the face down chip.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a face down mounted chip in the processes of Fogal as taught to be a useful method of attaching chips to a substrate in a multichip process by Kuranaga and Kuroga.

10. Claims 30 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Kuranaga and Kuroda as applied to claim 19 and 20 and further in view of Rostoker, and Takiar et al.

The combination of Kuranaga and Kuroda fails to teach a second chip mounted face down to the substrate, and fails to teach a stack chip bridging the two face down chips.

Rostoker teaches two face down chips attached to a substrate(fig 4a), and a stack chip bridging the two face down chips. Rostoker fails to teach the stack chip attached back to back with the face down chips.

Takiar et al teaches a face up chip bridging between two other face up chips(fig 9). Takiar fails to teach the base chips being attached face down.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to attach the second chip back to back in a process similar to Takiar and Rostoker as taught to be a useful method of attaching chips to other chips in a multichip process by Kuranaga and Kuroga.

11. Claims 32 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Kuranaga, Kuroga, Takiar et al, and Rostoker as applied to claim 30 and 31 and further in view of Fogal as applied to claims 21-29 and 33.

The combination of Kuranaga, Kuroga, Takiar et al, and Rostoker fails to teach a discrete die component and a second stacked die.

Fogal teaches two stacks of stacked chips, however, Fogal fails to teach the base chips being attached face down, or bridging the two stacks of chips.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to bridge the two stacks, and attach the base chips in a face down manner in the process of Fogal as taught to be a useful method of attaching chips to other chips in a multichip process by Kuranaga and Kuroga, Takiar et al, and Rostoker.

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Scott Kirkpatrick whose telephone number is (703) 305-7707. The examiner can normally be reached on Monday through Friday from 6:30AM-6PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling, can be reached on (703) 308-3325. The fax numbers for this group are (703)305-3599 and (703)305-3600.

Any inquiry of a general nature or relating to the status of the application should be directed to the Group Receptionist whose telephone number is (703) 308-0661.

GEORGE FOURSON
PATENT EXAMINER
GROUP 1100

Scott Kirkpatrick
January 5, 1997